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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,216	12/03/2003	Yong-Kyu Jang	8054-27 (LW8079US/WS)	5421

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,216	JANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,8,11-26,28,29,36-39,41,43,45,47-62,64-68 and 70-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-26,28,29,36,60-62,64-66,70 and 73-78* is/are allowed.

6)☒ Claim(s) *1-3,5,8,11-23,37-39,41,43,45,47-59,67,68,71 and 72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the Amendment filed 3 August 2006

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 11, 12, 15, 19-23, 37-39, 41, 45, 47, 48, 51, 55-59, 67, 68, 71, and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No 2003/0067570 to Okamoto et al. in view of U.S. Patent Publication No. 2002/0003596 to Kim.

Regarding claims 1, 19-22, 37, and 55-58, Okamoto discloses a liquid crystal display device (figures 23-28) comprising: a first substrate (29) including a TFT (21) formed thereon (figure 24); a first electrode (20) formed on the first substrate and electrically connected to the TFT (connected through 22, see paragraph 0437); a first insulating layer (25) formed on the first substrate including the TFT and the first electrode (figure 4), the first insulating layer having a window (opening at transmission display region 10) to expose a portion of the first electrode (see figure 24); a second electrode (19) formed on the first insulating layer and electrically connected to the first electrode (paragraphs 0436-0437) within the window along the periphery of the window (see figures 23, 24, and 28), the second electrode having an opening (see figure 24) to

expose the predetermined region of the first electrode, the window; a second substrate (62) including a third electrode (502) thereon (figure 27); a first gap between the surface of the third electrode and the predetermined region of the first electrode (see figure 27 – gap between electrode portion 20 and electrode 502 in the transmission region 10); and a second gap between the third electrode and the second electrode (figure 27 – gap between top of 19 and electrode 502 in reflection display region 9), wherein the gaps include a liquid crystal layer (1).

Okamoto fails to disclose that the color filter layer is continuously formed throughout the window region and the non-window region, but rather Okamoto discloses only partial coverage of the reflection window region by a color filter having the same thickness as in the transmission region, in order to provide sufficient brightness in the reflection mode (see paragraph 0455).

Kim teaches that a color filter substrate (110) may advantageously be formed by providing the color filter layer (130,132,134; alternately, 130a,b) continuously over the reflection and transmission regions (see figures 8, 9F, 10), where the color filter in the transmission region (window region) is twice the thickness of the color filter in the reflection region (non-window region; see paragraph 0051, 0075-0076), the thickness change being achieved by use of a thickness adjusting member (172, 190) upon which the color filter is disposed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the color filter substrate taught by Kim in the LCD device of Okamoto. The rationale is as follows: A person having ordinary skill in the art would note that Okamoto indicates that the goal of the color filter substrate is to achieve sufficient brightness and sufficient color integrity when functioning in the reflection mode (see Okamoto, paragraphs 0449-0455,0462). Since Kim indicates that a continuous color filter with a reduced thickness in the

reflection region advantageously achieves sufficient brightness and color integrity in the reflection mode, as required by Okamoto, and further provides the advantages of allowing for nearly identical brightness and color purity for both the transmission and reflection modes (see Kim, paragraphs 0031-0032), a person skilled in the art would have been motivated to use the color filter of Kim to achieve this uniformity.

Regarding claims 2, 3, 38, and 39, Okamoto discloses that the first electrode is a transmission electrode for transmitting light supplied from a source internal to the device, and the second electrode is a reflection electrode for reflecting light supplied from a source external to the device (see paragraphs 0429-0431; figures 24 and 27).

Regarding claims 5 and 41, Okamoto fails to specify the relative gap dimensions.

Kim teaches that the first gap is about twice as long as the second gap (see paragraphs 0014-0019, 0086).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the first gap in Okamoto be about twice as long as the second gap, as suggested by Kim. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide first and second gaps such that the first gap is twice as long as the second gap, because doing so ensures that the light from the reflection and transmission modes will have the same path length and phase, thus improving the performance of the device (see Kim, paragraphs 0014-0018).

Regarding claims 11, 12, 15, 47, 48, and 51, Okamoto discloses a gate driving circuit region and section (line 23 drives the gate of the TFT; see figures 23, 24, 28; paragraphs 0438-0439), wherein the insulating layer is absent only in the transmission display region (paragraphs 0436-0439; figures 23, 24), and wherein the gate driving line is not located in the transmission region (paragraph 0438), such that the insulating layer is present over the gate driving circuit (see figures 23-24).

Regarding claims 23 and 59, Okamoto discloses homogeneous alignment at a tilting angle of about zero degrees of the liquid crystal layer (see paragraphs 0205-0211).

Regarding claim 45, Okamoto discloses that the first conductive layer is made of ITO (paragraph 0436).

Regarding claims 67, 68, 71, and 72, Okamoto discloses that an end portion (portion of 19 contacting electrode 20) is formed on the first electrode exposed via the opening (figures 23 and 24), and wherein the window (region between insulating layer portions 25) is larger than the opening (region between bottom portions of 19; see figure 24).

3. Claims 8, 13, 14, 17, 18, 43, 49, 50, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto et al. in view of Kim, as applied to claims 1 and 37 above, and further in view of U.S. Patent No. 6,295,109 to Kubo et al.

Regarding claims 8, 13, 43, and 49, Okamoto as modified by Kim fails to disclose that the insulating layer is a photosensitive acryl resin having a thickness in the range of 0.5 microns-2.5 microns.

Kubo discloses that the insulating layer is a photosensitive acryl resin having a thickness of 2.5 microns (see column 49, lines 50-55; column 50, lines 10-20), where the photosensitive acryl resin has a lower dielectric constant than the liquid crystal layer measured in a parallel or perpendicular direction.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the LCD structure of Okamoto as modified by Kim, such that the first insulating layer is a photosensitive acryl resin having a thickness of 2.5 microns, as taught by Kubo. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a photosensitive acryl resin, because doing so allows for the reflection irregularities to be directly patterned into the insulating layer, without the need for additional photoresist deposition and removal steps, thus decreasing the cost and complexity of fabrication, as is appreciated by one skilled in the art (also see Kubo, column 49, lines 49-55). Since Kubo shows that a photosensitive acryl resin having a thickness of 2.5 microns provides the advantage of enabling direct patterning of the insulating layer while retaining properties suitable for use as an LCD insulation layer, it is well within the purview of a person skilled in the art to select such materials.

Regarding claims 14, 17, 18, 50, 53, and 54, Okamoto discloses an LCD structure including a TFT having a gate layer (23), source and drain layers (22 and 28), and a layer

between the two that is understood to be a gate oxide layer, where the gate oxide layer extends over the entire pixel array (see figure 24). Okamoto, however, does not specifically state that the layer overlying the gate line and provided under the transmission electrode (20) in the transmission display section is properly interpreted as an insulating layer.

Kubo shows a TFT structure substantially similar to that of Okamoto wherein a gate oxide layer (54, acting as the "second insulating layer") is provided on the first substrate, and includes a contact hole (portion 'at' item 66 of figure 29a), wherein the first electrode is connected to the TFT in the contact hole (see figure 29a). Since the gate oxide layer is only removed at the transmission window, it extends into the gate driving circuit region and over gate lines 53 (also see column 55, lines 52-60),

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the LCD of Okamoto as modified by Kim, by including a second insulating layer, as suggested by Kubo, such that the first electrode and TFT are connected through a contact hole in the second insulating layer, as further suggested by Kubo. The rationale is as follows: A person having ordinary skill in the art would recognize that a gate oxide layer must be present in a TFT in an LCD, as is illustrated by Kubo (see figure 29). Since Kubo further illustrates that the gate oxide layer can be used to control the point of connection between the source/drain electrode of the TFT and the transmission electrode of the pixel, thus preventing any shorting between electrodes or the TFT active region, a person skilled in the art would use the TFT structure taught in Kubo to provide the gate oxide layer and control the interconnections between the electrodes.

4. Claims 16 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto et al. in view Kim, as applied to claims 15 and 51 above, and further in view of U.S. Patent Publication No. 2003/0071944 to Baek.

Okamoto as modified by Kim fails to teach that the gate driving circuit region is formed from amorphous silicon.

Baek discloses that the gate driving circuit region is formed from amorphous silicon (paragraphs 0045-0048).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate driving circuitry of Okamoto as modified by Kim, such that the gate line structure includes amorphous silicon, as suggested by Baek. The rationale is as follows: A person having ordinary skill in the art would have been motivated to include layers of amorphous Si in the gate line and gate driving circuitry, because doing so allows for good ohmic contacts between the metal gate lines and the semiconductor material of the TFT, while allowing for a reduction in the number of layer deposition steps and photolithography steps (see Baek, paragraphs 0016, 0020, 0027).

Allowable Subject Matter

5. Claims 24-26, 28, 29, 36, 60-62, 64-66, 70, and 73-78 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for allowance for claims is the specifically claimed lamination of insulating layers and electrodes, and particularly the limitations that the first electrode is provided on an insulating layer covering the TFT, and that the second electrode does not contact

the first electrode at the contact hole (claims 24 and 60) or that it does contact the first electrode along a periphery of a window formed in the second insulating layer (claim 75), in addition to the other limitations in the claims.

The prior art of record including a first electrode formed on an insulating layer covering the TFT either teaches contacting the second electrode with the first electrode in the contact hole and not in the window (see US 6,620,655 to Ha et al. for example), or teaches structures wherein the first electrode does not connect to the TFT through a contact hole in the first insulating layer, but rather, connects to the TFT only through the second electrode (see US 7,015,996 to Sakamoto et al., for example). The prior art, however, provides no motivation for altering the contact structures such that the claim limitations are met.

Response to Arguments

7. Applicant's arguments with respect to claims 1-3, 5, 8, 11-23, 37-39, 41, 43, 45, 47-59, 67, 68, 71, and 72 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer M. Dolan
Examiner
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jmd

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